Claims

[c1] 1.An output driver for use with a random access memory array, said output driver comprising:
a clock generator for generating an output data path clock signal from a system clock signal, wherein said output data path clock is timed differently than said system clock signal; and
a programmable impedance system connected to said clock generator, wherein said programmable impedance system is timed according to said output data path clock signal.

[c2] 2.The output driver in claim 1, further comprising at least one level translator circuit connected to said programmable impedance system, wherein said level translator circuit comprises:
a level translator; and
a pair of latches connected to said level translator, wherein said latches are connected to said clock generator and are timed according to said output data path clock signal.

[c3] 3.The output driver in claim 2, further comprising a plurality of line driver circuits, wherein each line driver cir-

cuit is connected to a different memory line in said static random access memory array.

[c4] 4.The output driver in claim 3, wherein each of said line driver circuits comprises an output data latch, a pre-driver, a mid-driver, and a final stage driver.

[c5] 5.The output driver in claim 3, wherein all of said line driver circuits are connected to said clock generator and are timed according to said output data path clock signal.

[c6] 6.The output driver in claim 5, wherein because said level translation circuit is connected to said clock generator and said line driver circuits are connected to said clock generator, the timing of delivery of an impedance control signal from said level translation circuit to said mid-driver is coordinated with the timing of delivery of data from said pre-driver to said mid-driver.

[c7] 7.The output driver in claim 3, wherein said level translator circuit is connected to at least one of said line driver circuits.

[c8] 8.An output driver for use with a random access memory array, said output driver comprising:
a clock generator for generating an output data path clock signal from a system clock signal, wherein said

output data path clock is timed differently than said system clock signal;

a programmable impedance system connected to said clock generator, wherein said programmable impedance system is timed according to said output data path clock signal; and

a variable update circuit connected to said programmable impedance system, wherein said variable update circuit is adapted to control said programmable impedance system to perform impedance updates more frequently during initialization cycles than in cycles that occur after said initialization cycles expire.

[c9] 9.The output driver in claim 8, wherein said variable update circuit includes at least two differently timed clock dividers and a counter.

[c10] 10.The output driver in claim 8, further comprising at least one level translator circuit connected to said programmable impedance system, wherein said level translator circuit comprises:

a level translator; and

a pair of latches connected to said level translator, wherein said latches are connected to said clock generator and are timed according to said output data path clock signal.

[c11] 11.The output driver in claim 10, further comprising a plurality of line driver circuits connected to said clock generator, wherein each line driver circuit is connected to a different memory line in said static random access memory array.

[c12] 12.The output driver in claim 11, wherein each of said line driver circuits comprises an output data latch, a pre-driver, a mid-driver, and a final stage driver.

[c13] 13.The output driver in claim 10, wherein all of said line driver circuits are connected to said clock generator and are timed according to said output data path clock signal.

[c14] 14.The output driver in claim 13, wherein because said level translation circuit is connected to said clock generator and said line driver circuits are connected to said clock generator, the timing of delivery of an impedance control signal from said level translation circuit to said mid-driver is coordinated with the timing of delivery of data from said pre-driver to said mid-driver.

[c15] 15.The output driver in claim 11, wherein said level translator circuit is connected to at least one of said line driver circuits.

[c16] 16.An output driver for use with a random access mem-

ory array, said output driver comprising:
a clock generator for generating an output data path clock signal from a system clock signal, wherein said output data path clock is timed differently than said system clock signal;
a programmable impedance system connected to said clock generator, wherein said programmable impedance system is timed according to said output data path clock signal;
a plurality of line driver circuits connected to said clock generator, wherein each line driver circuit is connected to a different memory line in said static random access memory array; and
a plurality of level translator circuits connected to said programmable impedance system, wherein each of said level translator circuits is connected to at least one of said line driver circuits.

[c17] 17.The output driver in claim 16, wherein each of said level translator circuits comprises:
a level translator; and
a pair of latches connected to said level translator, wherein said latches are connected to said clock generator and are timed according to said output data path clock signal.

[c18] 18.The output driver in claim 16, wherein each of said line driver circuits comprises an output data latch, a pre-driver, a mid-driver, and a final stage driver.

[c19] 19.The output driver in claim 16, wherein because said level translation circuits are connected to said clock generator and said line driver circuits are connected to said clock generator, the timing of delivery of an impedance control signal from said level translation circuits to said mid-driver is coordinated with the timing of delivery of data from said pre-driver to said mid-driver.

[c20] 20.The output driver in claim 16, wherein all of said line driver circuits are connected to said clock generator and are timed according to said output data path clock signal.

[c21] 21.The output driver in claim 16, wherein each of said level translator circuits are connected to a plurality of said line driver circuits.

[c22] 22.A method controlling an output driver used with a static random access memory array, said method comprising:
generating an output data path clock signal from a system clock signal, wherein said output data path clock is timed differently than said system clock signal; and

timing a programmable impedance of said output driver according to said output data path clock signal.

[c23] 23.The method in claim 22, further comprising performing impedance updates on said output driver more frequently during initialization cycles than in cycles that occur after said initialization cycles expire.

[c24] 24.The method in claim 22, wherein said process of performing impedance updates utilizes at least two differently timed clock dividers and a counter.

[c25] 25.The method in claim 22, further comprising controlling the timing of a level translator according to said output data path clock signal.

[c26] 26.The method in claim 22, further comprising controlling the timing of a plurality of line driver circuits according to said output data path clock signal, wherein each line driver circuit is connected to a different memory line in said static random access memory array.

[c27] 27.The method in claim 22, wherein by timing said programmable impedance according to said output data path clock signal, the timing of delivery of an impedance control signal is coordinated with the timing of delivery of data.